ICOS
International Cooperation On Semiconductors

White Paper 2024

Generic Challenges and International Cooperation in the Semiconductor Field

A European Perspective

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This publication is part of the work executed in Workpackage 4 (Cooperation Framework) of the ICOS project.

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ICOS has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

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List of Acronyms

ATP	Assembly, Test and Packaging
CAGR	Compound Annual Growth Rate
CMOS	Complementary Metal-Oxide-Semiconductor
EDA	Electronic Design Automation
FD-SOI	Fully Depleted Silicon on Insulator
Fe-FET	Ferroelectric Field-Effect Transistor memory
FIT	Failures In Time: a reliability metric expressing the number of devices failing per billion operating hours
GaAs	Gallium Arsenide (a III-V compound semiconductor)
GaN	Gallium Nitride (a III-V compound semiconductor)
ICOS	International Cooperation On Semiconductors (a Coordination and Support Action funded by the Horizon Europe programme of the European Commission – grant number 101092562)
IDM	Integrated Device Manufacturer
InP	Indium Phosphide (a III-V compound semiconductor)
IP	Intellectual Property
IP-XACT	IP-XACT, also known as IEEE 1685, is an XML (Extensible Markup Language) format that describes electronic circuit designs
MOCVD	Metal-Organic Chemical Vapour Deposition (also called MOVPE – Metal-Organic Vapour Phase Epitaxy)
MRAM	Magneto-resistive Random Access Memory
OSAT	Outsourced Semiconductor Assembly and Test
PCRAM	Phase-Change Random Access Memory
PDK	Process Design Kit
PFAS	Per- and polyfluoroalkyl Substances
PIC	Photonic Integrated Circuit
RRAM	Resistive Random Access Memory
RTL	Register-Transfer Level: an design abstraction for digital electronic circuits
RTO	Research and Technology Organisation
SiC	Silicon Carbide (a compound semiconductor)
SiGe	Silicon Germanium (a compound semiconductor)
VC	Venture Capital
VCSEL	Vertical Cavity Surface-Emitting Laser

Executive Summary

Semiconductor technologies form the solid foundation of the digital economy, underpinning virtually every aspect of modern life, including communication, computing, health care, mobility, education, entertainment, online services, security, and more. As our reliance on electronic and photonic devices and infrastructure grows, the significance of semiconductors grows as well. The semiconductor industry has become a strategically critical industry. At the same time this is an industry of extremes: the chip making itself is done by a relatively small number of multinational industrial actors, in ultra-sophisticated and highly capital-intensive facilities and with the involvement of highly specialized personnel, and with a very uneven distribution across the globe. The technological innovation in the field evolves at a rapid pace and thereby matches the demand for ever more performant systems, but requires extraordinarily large investments in research, development, and fabrication facilities.

In this context there is a growing awareness and worry about the vulnerability of the semiconductor sector and the impact thereof on society at large. This worry manifests itself at a global scale where one recognizes that a major disruption in a semiconductor fab may have substantial worldwide implications in the many market sectors that depend on semiconductor devices. It also manifests itself at a regional or national level where governments and parliaments initiate actions to ensure that their region or country will be protected against supply chain shocks that would endanger their economy and the prosperity and welfare of their citizens. This is leading to a multitude of governmental initiatives, such as the "Chips Acts" in Europe and the US, in which regions or countries strive for a higher degree of autonomy or sovereignty with respect to the semiconductor supply chain. Such initiatives are of considerable magnitude and imply public funding, investment or loan, along with private investment, with a typical scale of several tens of billions of euro to strengthen the domestic manufacturing and R&D capacity.

Despite the increasingly vocal discourse on achieving chip sovereignty, international cooperation remains critically important in the semiconductor field for several reasons. First of all, the semiconductor supply chain has become highly complex and not only involves the actual wafer-level chip manufacturing but also the supply of advanced materials and manufacturing tools, the design capabilities and tools, the assembly, packaging and test methods etc. The strong driving force towards higher performance leads to higher sophistication in this supply chain. No single country or region possesses all capabilities and capacities to master the entire supply chain. Furthermore, most of the industrial actors are multinational anyway and semiconductor markets are inherently global. Secondly, the scientific and technological challenges that come with the push towards increased performance have a level of complexity that calls for collaborative research efforts involving scientists and engineers from around the world. Additionally, the increasing awareness about the environmental impact of the semiconductor industry opens up another large research field aimed towards cleaner and more energy-efficient manufacturing processes with the implementation of eco-friendly materials and technologies. These initiatives call for global cooperative action. Lastly, in an era marked by growing geopolitical tensions, international cooperation will, by itself, play a constructive role in fostering fair competition, trade and market access, benefitting consumers and industries worldwide. One could argue, perhaps optimistically, that the pursuit of sovereignty, which prompts increased investments globally and a more equitable distribution of capacity, can, when paired with international cooperation to tackle extremely difficult technical challenges and prevent redundant efforts, result in a robust, agile, and better-balanced global semiconductor ecosystem.

This whitepaper, developed within the context of the ICOS-project funded by the European Commission, sets itself the goal to spell out the generic challenges of the semiconductor field and the associated options to mitigate those challenges through international cooperation. The partners of the ICOS-consortium, encompassing key industrial, R&D and academic entities of the semiconductor field in the European Union, have identified fifteen such generic challenges. For each of them, the report discusses the main attributes of the challenge and proposes modalities of international cooperation that may be suitable to address the challenge and develop mitigating approaches. The whitepaper is written from a European perspective, but, as a result of the generic nature of the approach, its findings have a relatively universal significance.

Furthermore, the report may act as a source of inspiration to international stakeholders in the semiconductor field. For these reasons, the whitepaper is a public document.

As part of the work that led to the report, the European semiconductor community has been polled about the relative criticality of the fifteen identified challenges and of the need for international cooperation for each of them. All of these challenges were found to be at least somewhat critical. The top half of the resulting ranked list includes the following challenges (in order of priority): a. The dependence on non-EU chip manufacturers that may be subject to substantial risk of disruption; b. Risks or bottlenecks in the supply chain of goods for EU-companies; c. Critical dependence on one chip manufacturer (no second sourcing); d. Human resource challenges; e. Missing or outdated chip manufacturing infrastructure in the EU; f. Challenges with respect to the environmental impact of the semiconductor industry; and g. Foundry access and associated PDK[1] is missing.

Within the ICOS-project, the findings as presented in this whitepaper will be used, along with the in depth studies of the strengths and weaknesses of the semiconductor ecosystem in the EU and in other regions, to develop and prioritise concrete potential cases of international cooperation on specific subjects and with specific countries or regions. The outcome of this work will act as an input to the European Commission to initiate international cooperation agreements.

[1] PDK: Process Design Kit

Introduction and Methodology

The objective of the ICOS-project[2] is to support the EC in defining topics and measures to strengthen the position of Europe in the global value chain of semiconductor electronics and photonics, by focussed international cooperation initiatives with other leading semiconductor regions.

The present whitepaper report is part of the work executed in Workpackage 4 (Cooperation Framework) of ICOS. This Workpackage builds on inputs from Workpackage 2 (Economic landscape analysis of the EU and non-EU semiconductor value chains) and Workpackage 3 (Technology scanning and foresight) to:

1. identify generic needs and challenges in the semiconductor field for which international cooperation driven by public authorities is critically important and develop a prioritized list of such needs, and publish the results
2. identify potential cases of complementary cooperation with other countries/regions that address critical challenges or needs, both for the field of Advanced Computation and Advanced Functionality
3. prioritize these concrete cases by applying societal, environmental, economic, scientific and policy-driven filters

The present report addresses the first item of this list.

The work towards the whitepaper has progressed through three phases. Initially, the ICOS team identified a series of challenges faced by the semiconductor industry in Europe. Fifteen such challenges were pinpointed, with each accompanied by a breakdown of its key attributes and potential avenues for international cooperation. Subsequently, feedback on this list of challenges was gathered during an ICOS workshop held in Brussels on January 16-17, 2024. This feedback was not limited to the ICOS consortium but also involved input from the international and industrial advisory boards of ICOS. Further feedback was solicited from other European semiconductor stakeholders in the weeks following the workshop, facilitating a degree of prioritization in the process. Finally, the whitepaper report was composed and underwent three review cycles by members of the ICOS consortium, as detailed in the list of contributing authors.

[2] ICOS (International Cooperation On Semiconductors) is a Coordination and Support Action funded by the Horizon Europe programme of the European Commission – grant number 101092562. Project website: https://icos-semiconductors.eu/

Challenges and associated needs

ICOS has identified fifteen generic challenges for the European semiconductor industry and ecosystem. These are listed hereafter.

	Challenges – short name	Challenges – description
1	Manufacturing Fabs	Chip manufacturing infrastructure in the EU is missing or is outdated
2	Process Flow	Chip manufacturing infrastructure is available in the EU but process flow is missing or outdated/uncompetitive
3	Foundry Access	Foundry access and associated PDK are missing: a. globally; b. in the EU
4	Second Source	Critical dependence on one chip manufacturer (no second sourcing)
5	Disruption	Critical dependence on non-EU chip manufacturer(s) that are subject to substantial risks of disruption (commercial, environmental calamity, political, military, cyber risk…)
6	Competition	Competition from non-EU chip manufacturers is very strong
7	Workforce	Human resource challenges: insufficient skilled workforce, insufficient ability to attract talent, insufficient training and reskilling programmes, poor gender balance
8	R&D Capability	Insufficient availability of R&D capability in the EU or insufficient access to R&D infrastructure for technological POC and feasibility
9	IP-Core	Missing access to IP-core or other blocking IP issues
10	Supply Chain: Goods	Critical risks or bottlenecks in the supply chain of goods for EU-companies (materials, energy, gas, tools/equipment, other goods)
11	Supply Chain: Services	Critical risks or bottlenecks in the supply chain of services for EU-companies (services for EDA, assembly and package, test, other)
12	Investment	Insufficient investment capability (corporate and VC) across the supply chain, in particular for startups and SMEs
13	Export Restrictions	Commercial restrictions in the context of dual-use export control
14	Environmental Impact	Challenges with respect to the environmental impact of the semiconductor industry (energy, water, waste, chemicals, including PFAS)
15	Social & Governance	Challenges to meet social and governance goals, in particular social/political acceptance of major new initiatives.

For each of these fifteen challenges, ICOS has analysed the attributes of the challenge, possible options to mitigate it, with consideration of various dimensions (political, economic, social, technological, environmental and legal) and finally a preliminary list of cooperation options.

Challenge 1 Manufacturing Fabs

Chip manufacturing infrastructure in the EU is missing or is outdated

The first challenge relates to those semiconductor technologies or technology nodes where the EU lacks manufacturing infrastructure or where the available infrastructure is no longer at the state-of-the-art level. The ideal scenario would enable Europe to host comprehensive manufacturing capacities for all key semiconductor technologies[3], ensuring that European customers and industries have local access to these critical components through either foundry or IDM[4] models. Such autonomy would also localise control over technical and commercial strategies, primarily in European hands. However, the reality starkly contrasts with this ideal, highlighting a pressing need for infrastructure development.
Obvious examples of lacking infrastructure include the most advanced CMOS[5] nodes, even if the recently completed Intel Leixlip (Ireland) fab runs an Intel 4 node[6] and the planned Intel Magdeburg (Germany) fab will likely run an Intel 16A or 14A node[7]. Other companies, including TSMC, Infineon, NXP, Bosch, ST and Global Foundries, are also planning investments in Europe for CMOS nodes in the range 22 to 12 nm. Most of these investments rely heavily on public funding, as is typically the case for similar investments elsewhere in the world[8]. Public contributions originate from the European Chips Act and/or from national or regional funding bodies. Nevertheless, most of these new developments are still in the planning phase and the number of fabs for sub 28 nm nodes is still very limited in Europe.

While onshoring is the most direct and sovereign way to create chip manufacturing capacity in Europe, there may be factors that put forward near-shoring and friend-shoring as viable alternatives, on one hand for European chipmakers to establish a manufacturing supply chain and on the other hand for European customers to secure access to chip manufacturing. These approaches not only help mitigate risks but also support European manufacturers and consumers in maintaining a resilient supply chain. Given the large

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[3] Key semiconductor technologies include amongst others:
1. Advanced computing technologies such as: advanced logic technologies (multi-gate devices, nanowires, nanosheets, 3D integration, etc.), advanced memory technologies (charge-based and non-charge-based memories, including PCRAM (Phase-Change Random Access Memory), RRAM (Resistive Random Access Memory), MRAM (Magneto-resistive Random Access Memory), FeFET (Ferroelectric Field-Effect Transistor memory), neuromorphic computing, quantum computing, very low power technologies such as FD-SOI (Fully Depleted Silicon-on-Insulator), etc.
2. Technologies for advanced functionalities: smart sensing and actuation, smart power, communication, energy harvesting, semiconductor-based photonics, etc.
While silicon is the key semiconductor material in a majority of these technologies, there is a broad variety of other semiconductor materials that are critical for advanced performance or functionality, in particular compound semiconductors such as SiGe (Silicon Germanium), SiC and other group IV compounds; GaAs, InP (Indium Phosphide), GaN and other III-V compounds; II-VI and IV-VI compounds; 2D materials, etc.
Apart from monolithic wafer-scale processes, heterogeneous integration and advanced packaging also constitute important semiconductor technologies.

[4] IDM: Integrated Device Manufacturer

[5] CMOS: Complementary Metal-Oxide-Semiconductor

[6] https://www.intel.com/content/www/us/en/newsroom/news/new-fab-ireland-high-volume-production-intel-4-technology.html#gs.5stci1

[7] https://www.intel.com/content/www/us/en/newsroom/news/intel-german-government-agree-magdeburg.html#gs.5stjow

[8] As an example, one can mention the establishment by TSMC of 12 nm manufacturing capability in Japan, starting 2024, with public funding support from the Japanese government. https://pr.tsmc.com/english/news/3113

diversity in chip technologies combined with the enormous cost of establishing chip manufacturing infrastructure, it is unlikely that all possible flavours of semiconductor manufacturing will eventually be present in Europe. More and more, infrastructure investment initiatives will be multi-party initiatives, involving several medium- to large-size semiconductor companies, investment companies and public investment agencies, both from EU and from third countries.

For each initiative, these actors will do an in-depth analysis of all the relevant dimensions that will lead to the strategic decision of establishing the infrastructure in the EU, near the EU, in like-minded countries or elsewhere. These dimensions include amongst others economic and political factors, availability of skilled workforce and capability to attract skilled workforce, environmental boundary conditions, and more.

International cooperation will be critical in these large-scale endeavours. This cooperation will often have a public-private-partnership flavour. In the case of onshoring the public component will be mostly European, but the private component may be international. In the case of near- and friend-shoring there will also be an involvement of non-EU public authorities, in particular authorities that drive the public investment in innovation, in which case high-level political frameworks and agreements need to be established.

Challenge 2 Process Flow

Chip manufacturing infrastructure is available in the EU but process flow is missing or outdated/uncompetitive

Most process tools in semiconductor fab are versatile enough to support various manufacturing processes. Therefore, a given fab may well be capable of serving the manufacturing needs of multiple process flows and applications. For instance, a standard CMOS fab can adapt its process flow to create CMOS image sensors by incorporating additional modules for colour filters or microlenses. Another example is the silicon photonics chip, being a photonic integrated circuit (PIC) consisting of a variety of photonic components interconnected by ultra-compact optical waveguides. They are typically produced in a 90nm, 65nm or 45nm CMOS fab. Such PICs are essential for ultra-high-bandwidth transceivers that convert electrical signals to modulated optical signals transported over optical fibre, as needed for data centre applications and telecommunication networks. Increasingly they are also serving a variety of sensing applications, such as LIDAR and biosensors for medical diagnostics.[9] Other examples include the compound semiconductor technologies based on SiC[10] and GaN[11] (for high power or high frequency applications) or GaAs[12] (e.g. for VCSEL[13] applications). In these technologies it is less obvious to have a fab in which several semiconductor materials coexist, but there are cases where a CMOS fab has been converted into a SiC or GaN fab.

However, developing a process flow for new applications in a semiconductor fab is both capital- and labour-intensive, even when the depreciation cost of the fab infrastructure is not considered. The same may hold when the materials used in the process flow need to be changed, a recent example being the transition to PFAS[14]-free process flows. Typically, many hundreds to thousands of wafers need to be processed and evaluated through dedicated metrology, especially if the flow includes steps with unusual or very tight

[9] X-FAB is currently coordinating a CHIPS-JU project "photonixFAB" (grant agreement no. 101111896). The project is geared towards the establishment of an industrial process flow for silicon photonics, both for silicon nitride based PICs (in cooperation with Ligentec) and for silicon-on-insulator based PICs (in cooperation with imec).
https://www.photonixfab.eu/

[10] SiC: Silicon Carbide

[11] GaN: Gallium Nitride

[12] GaAs: Gallium Arsenide

[13] VCSEL: Vertical Cavity Surface-Emitting Laser

[14] PFAS: Per- and polyfluoroalkyl Substances

specifications. Additionally, the creation of an associated process design kit (PDK), which includes gathering extensive data on component variability and building compact models, is also resource-heavy.

Semiconductor fabs are often hesitant to engage in such an investment due to the high risks associated with uncertain market demands and fierce competition. This reluctance is exacerbated by potential gaps in technical knowledge and expertise needed for emerging products. In all those cases, there are several options to mitigate or spread the risk. These include cooperation with research and technology organisations (RTOs), possibly with partial public funding support, or industrial cooperation within or outside Europe (joint development programme, technology transfer, joint venture…).

Ecosystem and supply chain development may be crucial in this context, because it can make the difference in establishing first customer relations for the new product. Especially in those cases where the customer is not familiar with chip technologies or where the semiconductor fab has little affinity with the application, a concerted action involving all stakeholders in the supply chain (design, chip manufacturing, packaging, assembly and test, product development) may be of critical importance to lower the risks, the burdens and the barriers. Training and knowledge transfer is an important ingredient here, not only at the level of the technical experts in the respective organisations, but also in the board rooms as well as in educational programmes, both at vocational and academic level. Efficient dissemination to a broader public, starting with the end users' clients and expanding to encompass the general public, is equally crucial. Such ecosystem and supply chain development calls for an involvement of public and political stakeholders. Such collaborations not only reduce risks but also help in establishing initial customer relationships which are essential for market entry.

Training and the transfer of knowledge across organisational and educational levels play a critical role in the adaptation of new process flows. This not only applies to technical staff and engineers but also to management and decision-makers who need to understand the intricacies and potential of new technologies.

To keep up with the evolving landscape, especially when supply chains and production lines are globally interconnected, international cooperation becomes indispensable. It is particularly crucial for setting new standards[15] that accommodate innovative applications and technologies. This is particularly true at the interplay between chip design on one hand and packaging, assembly and testing on the other. There is, currently, significant competition in the standardisation of chiplet technology, with many initiatives in parallel, even in Europe. China has already launched its own standard tuned to the capabilities of its own supply chain[16]. The application may also impose new standards that are not yet common in the semiconductor industry (such as uncommon temperature ranges, uncommon wavelengths of operation in case of photonic devices, uncommon power consumption levels, uncommon FIT[17]-levels etc.). Also, the development of a skilled workforce for a new semiconductor technology can be a focus of international cooperation, e.g. through joint courses, trainings etc.

Challenge 3 Foundry Access

Foundry access and associated PDK are missing: a. globally; b. in the EU

This challenge is somewhat related to the previous ones, but focuses on the difficulty that a fabless company may face in accessing industrial manufacturing capacity for a given semiconductor technology. Especially for

[15] In the semiconductor field the main international bodies that develop standards are SEMI and IEEE. In Europe, there is no standardisation body that is specific for semiconductor technologies but there are broader-ranging bodies such as CENELEC (electrical engineering), ETSI (telecommunication) and CEN (other technical fields).

[16] https://www.linkedin.com/pulse/china-releases-its-own-chiplet-small-chip-standard-focusing-optimization/

[17] FIT: Failures In Time: a reliability metric expressing the number of devices failing per billion operating hours

new innovative technologies, it is not uncommon that capacity exists at the prototyping level – often offered by R&D players – but that industrial manufacturing only exists in captive mode or IDM-mode. Hence, there is a deficiency in pure-play foundry access. For the fabless company, such a lack of access is in essence a barrier for innovation, since the lack of an upscaling route for the given technology can easily put the company off with respect to this innovation track.

Even if foundry access exists, the financial barriers to use the foundry at the R&D and prototyping level may be very high. This is why most – but not all – foundries offer a Multi-Project-Wafer (MPW) modality, whereby the reticle area, as well as the cost of masks, wafers and processing are shared by multiple customers and each receives a limited number of chips. For small- and medium-sized companies, this MPW offering is critically important. This also means that the actors that act as broker and aggregator between the fab and the many users of the MPW-service have a critical role. In Europe, this role is successfully executed by actors such as Europractice[18], Imec.IC-link[19] and CIME-P[20]. For very advanced CMOS nodes (5nm and beyond) even an MPW-modality is excessively expensive for the user, both in terms of the fabrication and the design process, and there is a concern that such nodes are only accessible for a limited number of large companies, very few of which are European.

One can distinguish here between lack of foundry access at a global level or at an EU level. A foundry access outside Europe may well serve the needs of the fabless company, but it may be more prone to disruption than a foundry access in Europe.

The options to create an access route to a foundry or to a foundry-like service are manifold. A fabless company (or group of such companies) can lobby with both private companies and public bodies to invest in a foundry operation. They can also explore with IDMs the possibility to open up a foundry modality for an already existing process flow. This is consistent with the fact that, from the semiconductor fab side, the boundaries between foundry and IDM are blurring. Intel for example, which traditionally a pure IDM, has announced in 2021 to also deliver foundry services (Intel Foundry Services or IFS[21]). Recently this service has been rebranded as Intel Foundry[22]. To avoid conflicts, Intel strictly splits the foundry operation from the product operation, at least at the level of the sales organisation.

Another option to create foundry access is to strengthen the manufacturing readiness level (MRL) of a foundry-like offering in an R&D institute so that it will go beyond prototyping level and move into at least small volume manufacturing. The market volumes of some specialist semiconductor technologies are very well matched by what is considered low volume manufacturing in the semiconductor industry. An annual manufacturing volume of the order of 1000 wafers, considered small volume in the semiconductor industry, may translate into a million chips, which is considered medium to high volume in some application areas (such as special instrumentation, space applications, advanced medical instruments etc.).

On top of the options mentioned for Challenge 1 and 2, international cooperation can play an important role to establish access to a semiconductor technology. Fabless companies can work together to build a critical mass for such access and thereby make it commercially attractive for the fab to create a foundry operation, preferably with MPW modality.

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[18] https://www.europractice.com/

[19] https://www.imeciclink.com/en

[20] https://cime-p.cime.grenoble-inp.fr/

[21] https://www.intel.com/content/www/us/en/newsroom/news/intel-launches-1-billion-fund-build-foundry-innovation-ecosystem.html#gs.5r19z0

[22] https://www.intel.com/content/www/us/en/newsroom/news/foundry-news-roadmaps-updates.html#gs.5r1j3k

Challenge 4 Second Source

Critical dependence on one chip manufacturer (no second sourcing)

When a key product of a European fabless company is built from chips for which there is only one chip manufacturer, the company is critically dependent on that manufacturer. This is increasingly common in the semiconductor world, not only for very advanced CMOS-nodes but also for specialty technologies with a smaller market. This dependence is a high-risk situation, which can even be life threatening for the company. This is a severe issue, especially when the semiconductor fab can be subject to major disruption (see Challenge 5).

A fabless company can take several measures to mitigate the problem to some degree. It can build a stock to reduce the impact of temporary supply problems or it can proactively explore different technical solutions for the same product functionality and performance, and invest in prototyping runs for that alternative approach.

The issue is broader than this direct dependence of a fabless company on one chip maker. More generally, all European customers of that fabless company may also suffer, irrespective of whether the fabless company is in Europe or not. This broadens the problem considerably, since the scale of the economic sectors that depend on chips is simply massive.

International cooperation can be of crucial importance here, especially if the fab is outside Europe, to establish strategic ties and agreements with the company with an objective to limit the risks of the critical dependence. This will be discussed in more detail under Challenge 5.

A last resort is obviously to establish a new fab altogether, either in Europe or elsewhere, so that there are at least two players for the given technology. This is actually very similar to what was discussed in Challenge 1 and therefore the options are also very similar.

Challenge 5 Disruption

Critical dependence on non-EU chip manufacturer(s) that are subject to substantial risks of disruption (commercial, environmental calamity, political, military, cyber risk…)

Given the relatively limited choice of manufacturing fabs for many semiconductor technologies – especially advanced CMOS-nodes and specialty technologies – the risk of major disruption in a fab is one of the most worrying challenges for the European industry. There can be many possible reasons for such a disruption. The owners of the fab may decide to change the strategic direction of the company, especially at times of acquisitions or mergers. Or there can be environmental calamity such as earthquake[23], flooding, nuclear accident etc. This may not only happen at the site of the fab but also in a wider region and thereby disrupt the provision of energy, gases, water or other goods to the fab. Recent global events have also magnified the fear for disruption as a result of political or even military conflict[24]. In recent times, the occurrence of cyber-attacks on industrial manufacturing infrastructure has also increased. On the personnel side, a pandemic can

[23] The 7.2 magnitude earthquake that struck Taiwan on April 2 2024 appears to have caused relatively little disruption but reminds us of the enormous impact an earthquake could have in a region that has a global market share in chip manufacturing of more than 50%.

[24] Examples include Russia's invasion into Ukraine, the China-Taiwan tensions, the tensions in the strategic strait of Hormuz and more generally those in the Middle East.

disrupt the operation of a fab seriously. Finally, even if it is less common in the semiconductor industry than in other industries, social conflict may lead to strikes that also disrupt the operation.

Among the options to mitigate this challenge one can mention: strengthening and extending the production capacities of the European semiconductor manufacturers, preferably in Europe, and creating attractive conditions for non-EU manufacturers to establish capacity in Europe or in regions that are less prone to the disruptions mentioned earlier. The latter will call for international cooperation. If new fabs are to be built, a large-scale investment will be needed with involvement of private and possibly also public stakeholders. However, there is also considerable potential for strategic partnerships that may help to soften the impact of a major disruption. Two (or more) fabs could for example, encouraged by their customers and supported by public authorities, set up agreements to develop degrees of compatibility between their process flows, in such a way that the effort and cost needed to relocate the manufacturing of a given chip design from one fab to another are as limited as possible.

Cooperation between regions can also be of substantial importance here. Regions can work together and share their expertise to develop master plans on how to act in case of a major disruption and how to tap into mitigating measures. Joint supply agreements for critical materials or components may also hold important value.

Challenge 6 Competition

Competition from non-EU chip manufacturers is very strong

Any industrial chip manufacturing activity needs to be profitable to be viable. Today, Europe has a market share of less than 10% of the global semiconductor market, but aims to increase it to 20% by 2030 as a result of the Chips Act initiative. Given the strength of established fabs and foundries in Asia and in the USA, it is not obvious to grow market share, certainly not in those semiconductor technologies that are characterised by modest compound annual growth rate (CAGR).

This is where a global vision needs to be developed in the EU on strategic choices throughout the semiconductor value chain, with the aim to strengthen the capacity and the market share of the European semiconductor manufacturers to the benefit of European society at large. There are many dimensions to this strategic benefit for Europe and one must weigh many factors against each other when making choices between semiconductor technologies. Without striving for completeness, these questions include: what is the competitive picture? What is the investment needed (in infrastructure and in R&D cost) and what is the prospect for return on investment, not only in terms of revenue (market share) but also in terms of profit? What is the value for the European customer base? It is worth noting in this context that, while market share is a relevant metric, it is only a part of the value equation.

A combination of measures is needed: to invest in manufacturing infrastructure; to set up cooperations between RTOs and industrial companies on technologies with high growth potential, especially in those areas where Europe has strong markets; to build the workforce and to attract talent.

At the international level, partnerships and cooperation with key non-EU manufacturers can also be part of the strategy. Semiconductor companies may, even if they are competitors, identify win-win tracks of cooperation for part of their businesses. This may take the form of joint development of a process flow or even a joint venture for a particular manufacturing fab. However, in general terms, international cooperation may not be so easy with respect to competitive position and market share, because, globally speaking, market share dynamics is by definition a zero-sum game. However, there may well be cases where two regions join forces to boost their respective market shares – or at least their respective revenues - and do so in a cooperative mode. In other cases, one region may have a strong need to be customer for a particular type of semiconductor product, while another one has a focus on the manufacturing of these products. Such a

situation would be perfect for a win-win cooperation. Finally, in fast growing semiconductor markets it may be easier to set up cooperations, to meet the rising demand in a cooperative manner, than is the case in established and slower growing markets.

Challenge 7 Workforce

Human resource challenges: insufficient skilled workforce, insufficient ability to attract talent, insufficient training and reskilling programmes, poor gender balance

In view of the growth of the semiconductor market and the many investment initiatives resulting from the Chips Act in the EU as well as from similar initiatives in the US and in Asia, it is predicted that the talent shortage in the semiconductor ecosystem will become massive. Typical predictions for the global talent gap are of the order of 500,000 by 2030, of which approximately 100,000 in Europe[25,26]. The numbers for Europe are even larger when the ambition to reach 20% manufacturing share of the global semiconductor market is taken into account.

The problem will need to be addressed in two ways. First of all, by growing the talent base, by both reskilling (combined with strong retention methods) and increasing the influx of new skilled people, and then, by changing the work methods with stronger use of digitalisation.

The influx of new skilled people can be boosted in several ways. The most direct way is to grow the number of students in bachelor/master/PhD programmes that are relevant for the semiconductor field. To this end, education providers could for example increase the training options to include emerging fields, such as AI, quantum technologies, photonic chips etc., and advertise the evolutions in the semiconductor field along with their economic and societal relevance to prospective students. Creating a renewed message for the significance of the semiconductor industry towards achieving the Sustainable Development Goals[27], strengthening the brand recognition of the sector, is very important for the new generations. Education providers could also experiment with new teaching programme paradigms that deviate from the classical engineering programmes and that are more multidisciplinary or introduce innovative teaching methods. Attention to the broader context (geopolitical, environmental…) is a must in such programmes. Increased educational cooperation between academia and industry may also be very beneficial in this context. The continuation and extension of very low-cost EDA[28]-licenses for educational purposes may be very helpful.

The small fraction of students moving from secondary to higher education with an interest in technical studies acts like a limiting factor in this context. Boosting that fraction is challenging because it calls for STEM-oriented awareness programmes, especially towards girls, throughout primary and secondary education, with involvement of teachers and parents. The latter requires publicly supported initiatives involving many stakeholders. In many countries, there are only scattered and relatively small-scale initiatives. It may be worth bringing the issue to the political agenda and push for larger-scale and more concerted action.

Another way to grow the talent pool is to attract talent from abroad. This approach would better work for countries that have a surplus of skilled people relative to the absorption capacity of their own economy.

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[25] https://www2.deloitte.com/us/en/pages/technology/articles/global-semiconductor-talent-shortage.html

[26] https://www.mckinsey.com/industries/semiconductors/our-insights/how-semiconductor-companies-can-fill-the-expanding-talent-gap

[27] THE 17 GOALS | Sustainable Development (un.org)

[28] EDA: Electronic Design Automation

Attracting foreign workforce has many dimensions, not only salary, contract type and fringes, but also housing options, ease of administrative processes, cost of living, quality of life, work options for partner, school options for children etc.[29] From a cooperation point of view, while attracting foreign talent is convenient for a country, seeing the best talents leave the country is surely not. Talent rotation may be a balanced solution to this issue.

Retention and reskilling are the other part of the equation. This is a critical task for the HR-departments in the semiconductor companies. Already today, most of them are proactive in developing ways to let employees grow in their job, not just financially, but more generally in mid- and long-term professional development plans. An appreciative management style, flexible and smart working conditions, and more generally a company culture that one can be proud of, are all elements that matter. Last, not least, the employee should have ample opportunity to take time for reskilling through a variety of training modalities.

In terms of international cooperation, joint education programmes could be envisaged between an EU-university and a non-EU university (or multiple ones), including exchange options. For such exchange options, there would be a need for scholarships to cover the increased cost. Scaling such exchange programmes to relevant numbers is relatively expensive. To ensure political acceptance for such programs one may need to establish schemes for return on investment that are not only attractive to the investor in the programme (government and possibly also industry), but also to the students. This is a non-trivial challenge.

Apart from joint education, cooperation in the context of talent mobility and rotation could also be envisaged, as discussed earlier.

Challenge 8 R&D Capability

Insufficient availability of R&D capability in the EU or insufficient access to R&D infrastructure for technological POC and feasibility

With RTOs such as imec (Belgium), CEA-Leti (France), Fraunhofer (Germany) and others, Europe has a leading position in research in the semiconductor field. This is not only evidenced by the prominent contribution to publications in top-tier semiconductor journals and conferences[30], but also by the extensive degree of contract research executed for most of the leading semiconductor companies around the world. The R&D infrastructure of those institutions is primarily used for advanced research, but in specific cases it is also used for industrial prototyping and low-volume manufacturing, especially for those semiconductor technologies for which it can complement the industrial manufacturing capability.

Therefore, one may argue that there is not much of a challenge with the EU's R&D capability, including Proof of Concept (POC) prototyping for technology translation.

However, the key challenge is to maintain the leading position and use it, more than in the past, for the advancement of the EU's industrial semiconductor ecosystem and for the fulfilment of the objectives of the Chips Act. Given the enormous technical challenges and the rapid evolutions in semiconductor technology, and given the fact that other regions also start to invest more heavily in semiconductor R&D, it will indeed be a considerable challenge to stay at the forefront of the field.

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[29] This argument about the many dimensions that play when attracting non-EU personnel is also very relevant for mobility within Europe, especially because the semiconductor industry is somewhat clustered in a limited number of regions.

[30] As an example, about 18% of all papers at the 2023 edition of IEDM (International Electron Devices Meeting), considered one of the top conferences in the semiconductor field, had European contributions.

This is well recognized by the European Chips Act (adopted mid 2023), which, as part of its first pillar (the Chips for Europe initiative), aims to achieve large-scale technological capacity building and to support research and innovation activities throughout the EU chip value chain. The Chips Joint Undertaking (Chips JU) has been entrusted with the operational implementation of this pillar with a programme structure that includes both capacity building and R&I activities.

International cooperation has been very strong in the past, not only between RTOs and industrial parties, but also in between RTOs. This will likely remain in the future, but any cooperation will be influenced by the political reality of a stronger push towards sovereignty in different countries and regions of the world. This holds a certain risk for the global advancement of innovation in the semiconductor field, where scientific and technological complexity is at a scale that requires all global R&D capacities to work together.

In conclusion, Challenge 8 should perhaps be rephrased as: Consolidation of international cooperation in semiconductor R&D against a trend of increasing autonomy and sovereignty of the distinct countries and regions. The recently established digital partnership (signed in June 2023) between the EU and the Republic of Korea[31] is a commendable example of such consolidation.

Challenge 9 IP Core

Missing access to IP cores or other blocking IP issues

The semiconductor industry heavily depends on access to IP, especially on design IP in the form of IP cores (or IP blocks). In the digital electronics world highly mature methodologies have been established to turn core IP – both in soft and in hard form – into a commercial business. In Europe ARM (UK-based but majority owned by Japanese SoftBank) is one of the prominent IP-players with its RISC-based CPUs. In 2021 the global IP core market was estimated to be worth USD 4.58 billion.[32] Not only does this sector represent considerable economic value, but the access to IP cores is also strategically important. This is why Europe, and other regions, pay considerable attention to their position in the IP market. A two-tier approach with on one hand measures to grow the own IP-industry and on the other hand measures to ensure access to IP cores from other regions under fair and reasonable terms is a must.

The IP-business is expected to become more complex with the technological trend towards heterogeneous integration and chiplet integration. IP blocks will have the tendency to become more opaque, which carries risk for the users of the IP. These factors call for even more vigilant scrutiny of evolutions in the field.

In other (than digital) fields of semiconductor technology, such as analog and high-frequency electronic circuitry, the degree of IP-reuse is much less established, and also much harder, in part because abstractions and standards that are common in digital circuit design, such as RTL[33] or IP-XACT[34] (IEEE Std. 1685), cannot easily be translated to the analog world[35].The situation is even much worse in specialty semiconductor technologies such as MEMS or silicon photonics. There is probably very little design IP reuse in these fields across different IP-users, which is hampering their upscaling.

The challenges mentioned here are universal and not specific to Europe. This calls for international cooperation at various levels and between various actors. At the R&D level, one may work together to

[31] https://ec.europa.eu/commission/presscorner/detail/en/ip_23_3607

[32] https://www.fortunebusinessinsights.com/semiconductor-ip-market-106877

[33] RTL: Register-Transfer Level: a design abstraction for digital electronic circuits

[34] IP-XACT, also known as IEEE 1685, is an XML (Extensible Markup Language) format that describes electronic circuit designs

[35] As an example, IP-XACT supports analog and mixed-analog properties only since its recent IEEE Std. 1685-2022 version, published in 2023

develop new methodologies for design abstractions (including standards for, e.g., physical design planning) that enable IP reuse across many users and for IP blocks adapted to new technologies, such as chiplet and heterogeneous integration. In terms of IP operations, there is a lot to be gained from improved best practices for smooth and respectful licensing of IP cores (and more generally for any IP in the semiconductor field), especially in complex multi-actor cases. There may be an important role here for industry associations such as the European Semiconductor Industry Association (ESIA)[36] and the European Photonics Industry Consortium (EPIC)[37], along with the Association for European Nanoelectronics Activities (AENEAS)[38], the European Association on Smart System Integration (EPoSS)[39] and the Industry Association promoting on Intelligent Digital Systems (INSIDE)[40].

Challenge 10 Supply Chain: Goods

Critical risks or bottlenecks in the supply chain of goods for EU-companies (materials, energy, gas, tools/equipment, other goods)

The supply chain for goods essential to chip manufacturing is an integral part of the semiconductor ecosystem. Without this supply chain, there is no chip manufacturing. The chain includes materials, from raw materials and high purity materials in a wide variety of chemical compositions all the way up to ultra-precise wafers, photoresists, processing chemicals etc. High-purity gases and liquids, vital for numerous manufacturing steps, and energy carriers also play a critical role. In addition to these materials, the supply chain includes sophisticated equipment essential for chip manufacturing such as lithography tools, etching and deposition tools, cleaning and polishing tools, ion implantation tools, in-line testing and much more. Downstream from the chip manufacturing one finds tools for assembly, packaging and testing.

Europe's industrial strength in materials and tools is a bit variable. On one hand Europe has global 'heroes', such as for example Siltronic (Germany) and SOITEC (France) for wafers, ASML (The Netherlands) for deep-UV and extreme-UV lithography tools, and AIXTRON (Germany) for MOCVD[41] epitaxy systems. Also in the field of assembly and packaging, Europe has prominent tool vendors (Besi, Ficontec…). However, the scenario is less favorable in other parts of the supply chain. Only 2 of the top 15 equipment suppliers are headquartered in Europe. Furthermore, Europe's resources on raw materials are very limited and therefore Europe depends critically on other regions, in particular China, for this matter.

There is an obvious connection between material usage and environmental sustainability. This will be discussed in more detail under Challenge 14.

Given the simple fact that Europe depends on other regions for raw materials as well as certain types of equipment, while other regions depend on Europe for wafers and other types of equipment, there is potential for international cooperation between regions to allow them to address their respective gaps in a balanced way. This calls for a negotiation process with involvement of both public and private actors.

Apart from this, there are obviously many research questions that relate to materials and equipment geared towards better performance or better environmental sustainability. This calls for international research cooperation, as discussed under Challenge 8.

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[36] https://www.eusemiconductors.eu/esia

[37] https://epic-photonics.com/

[38] https://aeneas-office.org/

[39] https://www.smart-systems-integration.org/

[40] https://www.inside-association.eu/

[41] MOCVD: Metal Organic Chemical Vapour Deposition

Challenge 11 Supply Chain: Services

Critical risks or bottlenecks in the supply chain of services for EU-companies (services for EDA, assembly and package, test, other)

The market for EDA-tools and -services has traditionally been dominated by the US. The OSAT[42] (or ATP[43]) service market is mostly dominated by Asian countries. In both areas, Europe has a relatively small market share. In terms of EDA-tools this has changed somewhat since the acquisition by Siemens of Mentor Graphics in 2017. In the area of photonic chips, which requires dedicated EDA tools, one can distinguish on one hand large actors, such as US-based Synopsys, which have a photonics division, and on the other hand SME's, such as Europe-based Luceda Photonics, which focus entirely on photonic design tools. Both have a relevant market share. Assembly, packaging and test have been outsourced to Asian companies for decades. So, there is little capacity left in Europe. This is becoming a critical dependency at a time where packaging is gradually moving from die-level to wafer-level processing, to keep up with the demand for higher performance and lower cost, and where the field is moving from being innovation-light to innovation-heavy. In the photonics area, where packaging and assembly of PICs was traditionally considered to be challenging and costly, there has been a concerted effort through the Pilot Line project PIXAPP, coordinated by Tyndall, to develop more standardised approaches and to grow the industrial ecosystem. Several new European companies are active in this space, but most of them are not yet capable of performing packaging in high volume at low cost and rather focus on high precision packaging in modest volume.

It is unlikely that the relatively modest position of Europe in EDA-tools and in ATP-services can be drastically improved just by growing the existing industrial actors or creating new companies altogether. Therefore, a two-tier approach seems appropriate. On one hand the existing European actors should have the opportunity to strengthen their global competitive position and to develop new innovative tools or services in which they can establish a leading role. In parallel, the dependency on non-EU actors should be turned into an asset by encouraging those actors to establish substantial activities in Europe (which is already the case for Synopsys' photonics EDA activities) and by entering into bilateral cooperation and commercial agreements with such non-EU players to secure access to services and facilities not available within the EU ecosystem (redundancy & diversity).

One of the challenges in the EDA-field, from a designer's point of view, is that the transition from one vendor's software suite to another implies a lot of reskilling and cost. Therefore, it is risky to completely depend on only one vendor. This calls for the development of more standardised and more compatible EDA-tools. Open source approaches can also help to reduce the dependency on one EDA-tool vendor and may be particularly relevant for the academic community as well as in the context of training programmes on chip design (see also Challenge 7). For the latter – training – international cooperation can be instrumental to build high-quality training programmes with an as low as possible access barrier.

Challenge 12 Investment

Insufficient investment capability (corporate and VC) across the supply chain, in particular for start-ups and SMEs

[42] OSAT: Outsourced Semiconductor Assembly and Test

[43] ATP: Assembly, Test and Packaging

The capital available in Europe for deep tech investments has traditionally been much smaller than in the US or in Asia. This is true both for corporate investments in for example chip manufacturing capacity and for VC investment in start-ups that are users of or providers to the semiconductor ecosystem. In the past decade, Europe has gone through a catch-up process, but the gap remains considerable. The European Chips Act – through access to the Chips Fund – aims at reducing the gap further.

The establishment of chip manufacturing capacity has already been discussed under Challenge 1 and 2. From an investor's point of view, the key question is obviously whether the chances are good for a considerable return on investment, considering both the market prospects and the competitive situation. In this context, it is worth emphasizing that there is a wide spectrum of semiconductor technologies and therefore also of associated investment levels. At the most extreme end, there are the investments in new advanced CMOS nodes, where the combined cost of the infrastructure and the process development runs into the tens of billions of euro. At the other end of the spectrum, there are those semiconductor technologies that can be implemented in existing fabs with relatively minor modifications of the tool set needed for the process. Here the investment level can be orders of magnitude lower, down to tens of million euros. Especially in those cases where such a semiconductor technology is geared towards a rapidly growing market, the investment may be attractive to and may fit the scale of many more investment actors.

European VC investment into start-ups (and more generally into SMEs) is much larger today than it used to be one or two decades ago. The establishment of the Capital Market Union (CMU) by the European Commission has helped to create a single European capital market to the benefit of consumers, investors and companies anywhere in the EU.[44] One can now observe a vibrant community of innovative players, especially at the application end of the semiconductor value chain, but also in a wide variety of commercial service and provision activities, from EDA-tools and equipment to packaging and testing services. However, despite these gains, many deep tech start-ups continue to be underfunded, especially in comparison to their US counterparts, and often struggle to advance from development to scale-up phases due to difficulty in securing subsequent rounds of investment. The scale-up process is particularly daunting and requires substantial investments which many start-ups fail to secure, thus remaining at a subcritical size or folding altogether. The EU Chips Act is expected to partly mitigate this problem, since one of the objectives of the Chips for Europe initiative is to set up a Chips Fund to facilitate access to debt financing and equity, in particular for start-ups, scale-ups, SMEs and small mid-caps. This initiative will be implemented by the European Innovation Council and InvestEU.

How can international cooperation bring added value in this context? Foreign investment will obviously help to grow industrial activities in Europe. This has already happened in considerable degree in the past since European companies such as ASML, ARM, ASM, BESI and others are owned for a large part by non-EU shareholders. In parallel, large non-European companies such as Intel and TSMC invest heavily in European manufacturing infrastructure. In both situations the non-EU ownership reduces the degree of European sovereignty of the semiconductor ecosystem, but is nevertheless crucial in socio-economic context as well as to safeguard access to chip production for European customers. In the case of SMEs and start-ups, the access to non-EU VC investors is relatively challenging. There may be a role here for stronger public-private initiatives between regions outside EU and regions within EU that bridge between investment provision and investment need. Ideally, such initiatives would be balanced. The net result could be that SMEs and start-ups can more easily identify potential investors outside Europe.

Addressing the investment deficiencies in Europe's semiconductor sector requires a multifaceted approach involving enhanced local funding mechanisms, supported by international investments and collaborations. These efforts are vital for enabling European entities not only to compete on a global stage but also to drive technological advancements in the semiconductor industry.

[44] https://finance.ec.europa.eu/capital-markets-union-and-financial-markets/capital-markets-union_en

Challenge 13 Export restrictions

Commercial restrictions in the context of dual-use export control

Export control for dual-use products and technologies (as well as arms) is an important tool for maintaining international peace, stability and security as well as for the protection of human rights. In the current geopolitical climate, export restrictions have gained considerable importance. The basic rules of export control have been established, since 1996, in the Wassenaar agreement. Since then, 42 countries have signed the agreement, including amongst others the EU countries, UK, Switzerland, Norway, Turkey, Ukraine, USA, Canada, Japan, South-Korea, India, and Russia. The Wassenaar agreement aims to restrict the export of dual-use goods and technologies and to make these restrictions transparent, but does not spell out the detailed measures. That remains the privilege of the individual countries. Through the 2021/821 regulation the EU has set up a uniform export control regime that all EU countries comply with, at least in terms of the general principles. However, the detailed export control lists differ somewhat between individual EU countries.

For companies export restrictions will obviously restrict business and will therefore reduce the revenue and profit. Nevertheless, given that the export restrictions are set up in a democratic and transparent context, and with equal rules for all players within the EU as well as for those in like-minded countries, the industry will and must comply with them.

Strictly speaking, any semiconductor product is dual-use: it can be used both for civil and for military applications. However, export restrictions typically only apply to those products or technologies that allow for or can enable very advanced performance and that are not so easily accessible. These are considered sensitive or strategic products or technologies. It is a matter of judgment to decide which technologies or products fall under that category. Moreover, given the rapid pace of evolution in the semiconductor field these judgments need to be updated at just the same pace.

The challenges begin here: the detailed export control lists of individual countries are difficult to read and can easily become outdated due to technological evolution. Furthermore, companies with activities in multiple countries need to take into account the export control measures of the respective countries. Companies also wish to experience a fair and equal treatment relative to their competitors.

Export control laws have cascading effects. For example, any product that includes or is bundled with US-origin[45] items is subjected to US Export Control Laws, irrespective of the licensing conditions of these items. Because of the extra-territorial application of US Export Control Laws, these become a re-export control of products from one country to another. If a EU company is using US-origin items in its design or fabrication process, and if that item becomes barred from export to one country, then the EU company can no longer export its product to that country. This can lead to distortion of competition, in particular if the foreign country was a significant market for the EU company, and not so much so for non-EU based competitors.

All of this requires extensive cooperation, on one hand between the EU member states and on the other hand at an international level. Since 2021, the EU has already established a Trade and Technology Council (TTC) with the US, to align better the trade policies between the two regions. While the TTC covers a comprehensive set of trade and technology related issues, it also aims for better alignment on export control. More recently, in 2023, the EU established a TTC with India.

Apart from these country-specific actions, the European Commission also develops general strategies and measures on economic security and export control. In June 2023, the European Commission published a

[45] US origin is assumed for any item (commodity, technology, or software) contributed from a US national anywhere in the world, or from a foreign national on US territory.

Joint Communication on a European Economic Security Strategy[46], to minimise the risks to economic security in the context of increased geopolitical tensions and accelerated technological shifts, while preserving maximum levels of economic openness and dynamism. The EC White Paper on export controls[47] , published on 24 January 2024, aims to launch a discussion on the current EU export control system and sets out actions to address some of the existing gaps. These include in particular: to consider alternative approaches to introduce uniform EU controls for those items that have been agreed with partners at multilateral level, and, to create a forum for political level coordination on export controls between the Commission and Member States to foster common EU positions.

In spite of the restrictions set by export control, one should not forget that a big fraction of all products and technologies in the semiconductor field are not subject to such restrictions. This implies that trade continues to happen, not only between like-minded countries, at a large scale. It is often argued that this trade, especially if it is somewhat balanced and therefore creates mutual dependency, can also work as a counterforce against disruptions of international stability. This makes the judgment whether a certain product or technology should appear on the export control list even more difficult. When it is on the list, the product or technology cannot be abused for military purposes. However, when it is not on the list, creating a mutually valuable balanced trade could help. The choice is a political decision.

Challenge 14 Environmental Impact

Challenges with respect to the environmental impact of the semiconductor industry (energy, water, waste, chemicals, including PFAS)

The environmental cost of semiconductor manufacturing is substantially large. There is large energy consumption, large consumption of ultra-pure water, waste and greenhouse gas emissions, and the environmental cost rises with every new CMOS node. Imec, which has developed an open R&D programme on sustainable semiconductor technologies and systems (SSTS), estimates that the energy cost for manufacturing a 2 nm wafer is well above 1000 kWh and the CO_2-equivalent GHG emission goes beyond 300 kg for a wafer[48]. Moreover, the water withdrawal per wafer is of the order of several m^3. There are very considerable efforts now in the semiconductor industry to find ways to reduce the environmental impact. Newly built fabs score a lot better than older fabs (for the same node), but there still is a very long way to go.

The challenge will need to be tackled from many sides. From the technological and research side, one can prioritise for eco-friendly alternatives to hazardous and/or high environmental impact materials (e.g., PFAS, oil-based packaging...), fabrication and recycling processes. One can develop strategies to qualify non-harmful chemicals to substitute chemicals that lead to problematic wastes and contaminants. One can replace fossil fuel-based energy by sustainable energy. One can improve on water recycling methods.

However, technology alone will likely not suffice to tackle the environmental impact to a sufficient degree. There will also be a need for holistic life cycle analysis, including the use of EVR models (Eco-costs/Value Ratio) to reveal sustainable and unsustainable consumption patterns of people. It does not make sense to use very advanced and eco-costly CMOS-chips if they are used in a product that is discarded after a short period of time. It is a political choice to implement policies and regulations to discourage such consumerist usage. It is also a political choice to ban certain chemicals altogether or to set hard limits to the use of energy, water and other resources in absolute or relative terms.

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[46] https://ec.europa.eu/commission/presscorner/detail/en/IP_23_3358

[47] https://circabc.europa.eu/ui/group/aac710a0-4eb3-493e-a12a-e988b442a72a/library/a44df99c-18d2-49df-950d-4d48f08ea76f/details?download=true

[48] https://www.imec-int.com/en/articles/environmental-footprint-logic-cmos-technologies

International cooperation is probably more important for this challenge than for any other challenge discussed in this white paper. First of all, the technological challenges to reduce the environmental impact are enormous and therefore the importance of R&D cooperation cannot be overstated. Secondly, it is crucial to establish a level playing field in which competitors work by the same set of rules, also in terms of environmental cost. This will call for international alliances, such as the TTCs mentioned earlier, in which the semiconductor manufacturers comply with ambitious but realistic regulations and in which they agree to be transparent about their environmental cost. Within the boundaries of such alliances, trade can be freer than when crossing the boundary. Import restrictions may need to apply if certain regulations are not met, in a way similar to for example the regulations that exist for the import of ozone-depleting substances and fluorinated greenhouse gases.

Challenge 15 Social and Governance

Challenges to meet social and governance goals, in particular social/ political acceptance of major new initiatives.

Environmental, social and governance (ESG) aspects form the basis of corporate social responsibility. Up to the end of the 20th century, ESG was mostly driven by philanthropic individuals and there was a widespread belief that ESG could easily harm the financial return on investment of a company. Since then, the minds have changed up to a point where ESG is now considered the norm and where many companies have very explicit charters on good governance and on integrity, and where they spell out a Code of Conduct with respect to ethical behaviour for their employees. The semiconductor industry is no exception to this evolution. Moreover, it is now generally believed (and substantiated by recent studies) that companies with good ESG practices thrive better in the long run, also financially[49], even if such good ESG practices have a cost and therefore imply a competitive disadvantage in the short term. Europe appears to have a higher fraction of ESG leaders than other regions and a lower fraction of laggards.[50]

Here we focus mostly on the Social and Governance part, since Environmental aspects were covered under Challenge 14.

Despite the general positive evolution in ESG, there continue to be considerable challenges, as evidenced by the regular reports in the media about violations of good governance or of environmental regulations as well as about social conflicts. While the industry is to some degree self-regulating with respect to ESG, in particular because of the correlation between ESG and long-term return on investment, further progress would benefit from incentive-based public policies, either through tax incentives or through public funding incentives that depend on ESG performance. This calls for an independent and neutral body, at EU-level or even global level, that can assess this performance through well-defined criteria and metrics. The common critique that companies can easily deceive through window dressing and green washing should be addressed through such well-chosen metrics, like the solid approaches used for financial reporting.

The semiconductor industry is following the general trends in the economy in this context. In view of the strong dependence of Europe on other regions – and given Europe's leading role in ESG one can argue that the European industry has a competitive disadvantage for short-term revenue and profit. Therefore, it is very

[49] https://www.kroll.com/en/insights/publications/cost-of-capital/esg-global-investor-returns-study

[50] Quote from the above study: "In December 2021, nearly a third of Western European companies were rated as ESG Leaders and only 6% (= 122 / 1,929) were considered Laggards. In contrast, only 10% of North America and 6% of Asia companies enjoyed a Leader rating. North America and Asia also saw a greater proportion of Laggards, at 17% and 38%, respectively."

important to bring ESG goals to the table of any international negotiation or plan for cooperation, so that a more uniform level playing field can be established.

Major infrastructure initiatives, such as the building of a large new fab, can easily lead to resistance by local residents, because of the environmental impact. Large initiatives therefore require in-depth study of appropriate locations and of the effects on the environment, in close collaboration with local authorities, as well as extensive and effective communication with the local community. International cooperation is typically not at stake here, except of course in those cases where an EU-company takes the initiative to friendshore or offshore a fab outside the EU.

Prioritisation

It is not the purpose of this document to come to a strict prioritisation of the fifteen challenges. This should rather be done at a more specific level that also takes into account specific technologies and cooperation with specific regions.

Nevertheless, ICOS conducted a small-scale survey among experts from the European semiconductor field to get a feel for the perceived severity of the respective challenges as well as for the perceived need for international collaboration. For each of the challenges two questions were asked in this survey:

1. How critical is the challenge for Europe?
2. How critical is international cooperation for the challenge?

For each of those two questions four possible answers, could be given: not so critical, somewhat critical, very critical, most critical.

The survey was done in two steps. In a first step the participants of the ICOS-internal workshop in Brussels on January 16-17, 2024 were polled in real time (using the online Miro-tool). The workshop was attended by representatives of the ICOS-consortium (in particular the work package and activity leaders) as well as by representatives from the European Commission and from the Industrial and International Advisory Boards for ICOS. In total, 32 persons responded. The survey was transparent during the real-time polling but anonymous afterwards in the sense that the identity of the respondents was not logged in Miro. The real-time nature of the polling obviously implied that the participants provided a very spontaneous and intuitive response. The results of the poll were visible on screen during the polling, meaning that one could be influenced by the already visible result.

In a second step, the survey was sent out to a broader group of people using the online tool Qualtrics. This group included all people involved in the ICOS-consortium as well as members of the Management Committee of AENEAS. They were all given several weeks to respond, meaning that they had much more time to reflect about the questions than in the Miro-polling. The survey was anonymous, but the participants were requested to spell out the type of organisation they belong to (industry, RTO, university, other). 22 persons responded, of which 12 from industry, 5 from RTO's or universities and 5 other. It is quite possible that some members of ICOS responded twice, once during the workshop and once during the offline polling. These persons have therefore had a double voice.

The results of both surveys are shown in Figure 1. For each challenge the standard deviation ellipses are provided in the two-dimensional space drawn by both questions. The ellipticity provides an indication for the correlation between the answers to both questions and the orientation of the ellipse for the type of correlation. The results are plotted on one hand for the real-time Miro-poll (labelled as "ICOS-workshop") and on the other hand for the respondents to the Qualtrics-poll, split out and labelled by "Industry", "RTO+University" and "Other" respectively.

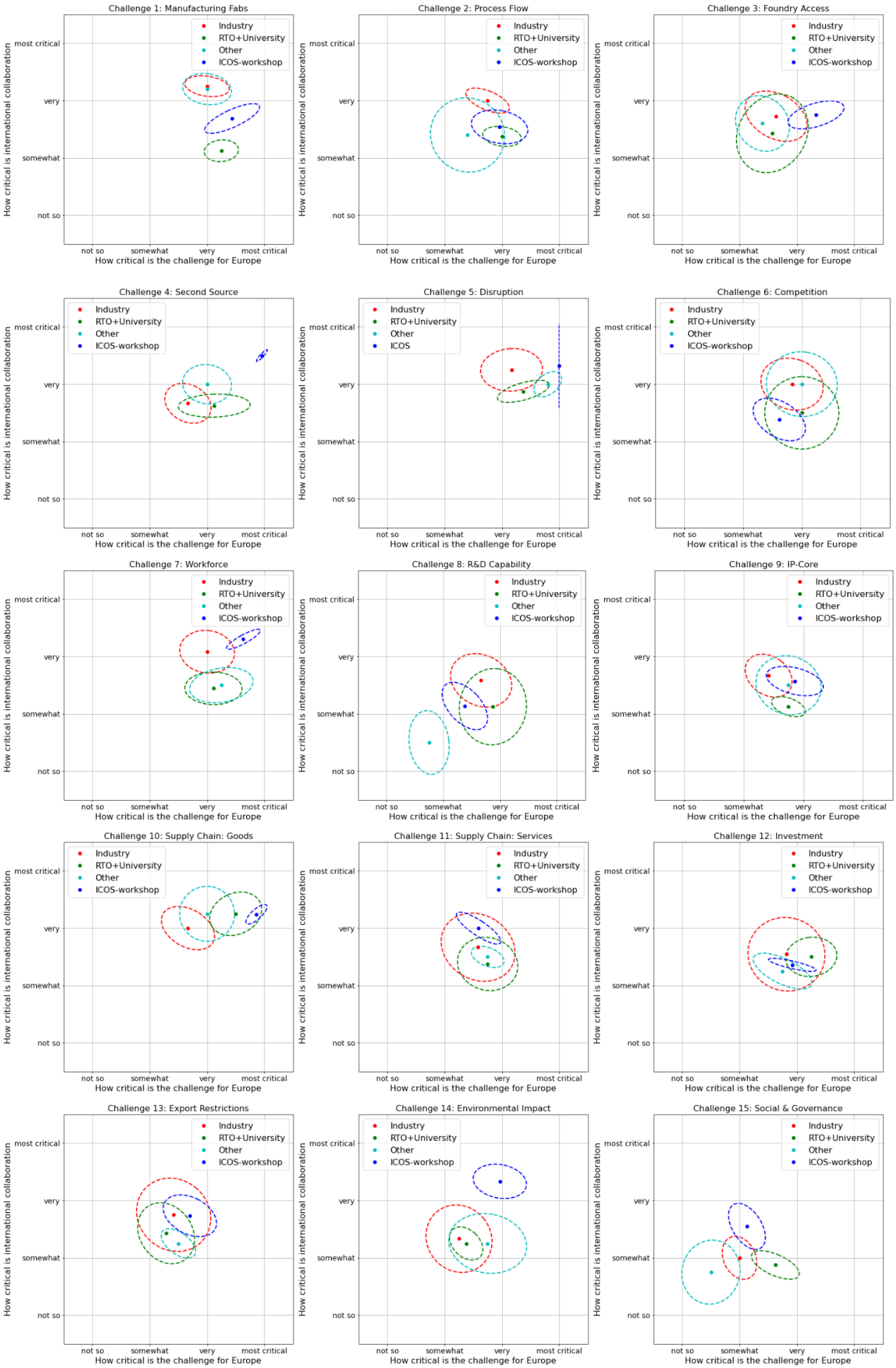
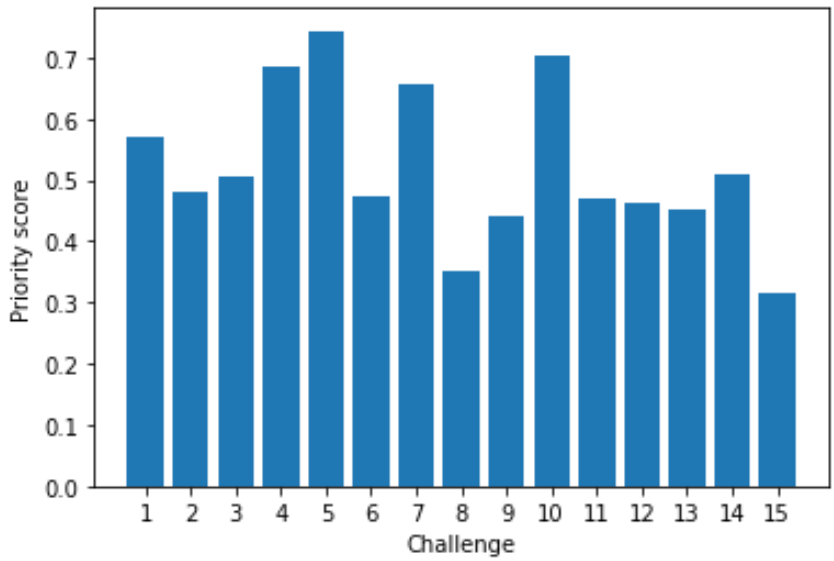


Figure 1 *Statistical standard deviation ellipses for the responses to the survey about the fifteen challenges.*

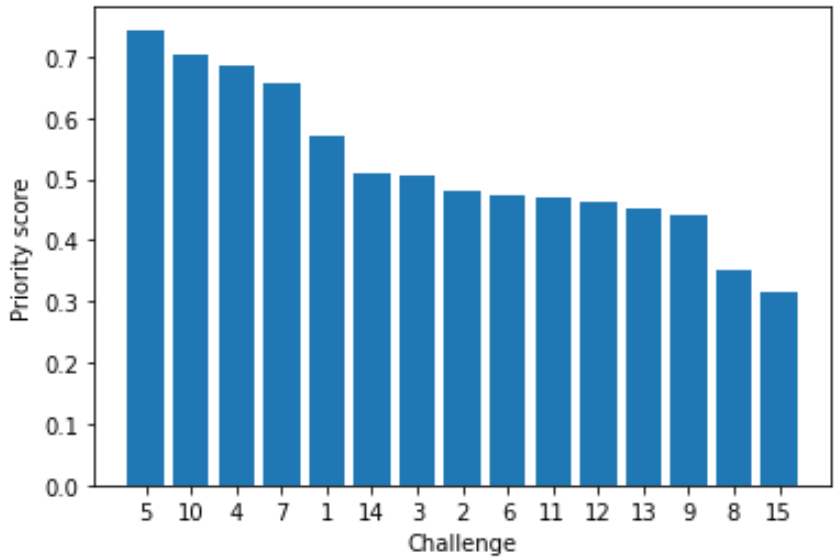
The discrepancies between the opinions of the different groups are relatively modest. In many cases the ellipses overlap substantially. There are a few outliers, in particular between the results provided by the workshop participants and those provided offline. This may well be due to the fact that in a workshop one can easily be influenced by the presentations presented in advance of the polling and by the fact that one could be influenced by the transparent online polling.

As a final exercise, we derived a priority ranking from the data. For both dimensions (criticality of challenge and criticality of cooperation) a score of 1,2,3 or 4 was given for the four possible answers (1: not so critical; 4: most critical). Then, the product was taken of both scores, resulting in a score between 1 and 16. After averaging over all respondents and normalisation between 0 and 1, we obtained Figures 2 and 3. In Figure 2, the priority score is given for each of the challenges. In Figure 3, the same information is shown, but ordered by priority. One can see that there is a top group of five challenges that stand out. These include:



1: Manufacturing Fabs
2: Process Flows
3: Foundry Access
4: Second Source
5: Disruption
6: Competition
7: Workforce
8: R&D Capability
9: IP-Core
10: Supply Chain: Goods
11: Supply Chain: Services
12: Investment
13: Export Restrictions
14: Environmental Impact
15: Social & Governance

Figure 2 Normalised priority score for each of the 15 Challenges, in the context of international cooperation.



1: Manufacturing Fabs
2: Process Flows
3: Foundry Access
4: Second Source
5: Disruption
6: Competition
7: Workforce
8: R&D Capability
9: IP-Core
10: Supply Chain: Goods
11: Supply Chain: Services
12: Investment
13: Export Restrictions
14: Environmental Impact
15: Social & Governance

Figure 3 Same information as in Figure 2, but ordered by priority score.

Disruption, Supply Chain: Goods, Second Source, Workforce and Manufacturing Fabs.

This is followed by a larger group of 8 challenges with more or less equal score. These include: Environmental Impact, Foundry Access, Process Flows, Competition, Supply Chain: Services, Investment, Export Restrictions and IP-Core. Finally, the two challenges R&D Capability and Social & Governance receive the lowest priority score.

Outlook

The generic framework outlined in this whitepaper serves as a tool within ICOS for pinpointing specific instances of international cooperation in the semiconductor domain, encompassing technologies for advanced computation and advanced functionalities alike. Input will be solicited from both industry and R&D organisations. Following this, filters will be established to prioritize these cases, considering various dimensions such as societal impact, economic feasibility, alignment with EU policy, and environmental considerations. Leveraging these filters, cooperation cases will be ranked through engagements with a spectrum of EU stakeholders, including public authorities, industry representatives, societal actors, and the R&D community.

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ICOS has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.