Institute of Engineering and Management of Grenoble Alpes University

HR EXCELLENCE IN RESEARCH

Grenoble INP - UGA is a member of **international** engineering and management education and research **networks.** It is widely recognized in national and international rankings**.**

8 schools + **39** laboratories

8300 students

1 300 teaching, research, administrative and technical staff

Grenoble INP-UGA is a renowned public institution of higher education and research, and a major player in the Grenoble ecosystem. It is the engineering and management institute of Grenoble Alpes University, and plays a leading role in the scientific and industrial community.

University Associate Professor Position

Short profile	Digital Electronics
Body	University Associate Professor
Position number	61-63 MCF 0462
CNU Section	61-63
Location	Grenoble
Date of recruitment	01/09/2023
Key words	Frugal digital electronics, embedded systems design, digital architecture design in disruptive technologies

Grenoble INP - UGA is a leading public institution accredited with the French label "*Initiative d'excellence*". It offers innovative engineering and management programs, with an increasing internationalization of its course offers. The courses are grounded in sound scientific knowledge and linked to digital, industrial, organizational, environmental and energy transitions. The Institute of Engineering and Management of Grenoble Alpes brings together more than 1300 staff members (teacher-researchers, lecturers, administrative and technical staff) and 8300 students, located on 8 sites (Grenoble INP - Ense3, Grenoble INP - Ensimag, Grenoble INP - Esisar, Grenoble INP - Génie industriel GI, Grenoble INP - Pagora, Grenoble INP - Phelma, Polytech Grenoble, Grenoble IAE and the INP Prepa). Grenoble INP is also a highly-ranked institution of higher education and research, one of the leaders in the fields of engineering and management at international level. It is one of the members of the European University UNITE!, which comprises a large number of international academic and research partners.

As part of Grenoble Alpes University, Grenoble INP is associated to 40 national and international research laboratories and technological platforms. Grenoble INP is at the heart of the following scientific fields: physics, energy, mechanics and materials; digital; micro and nano-electronics, embedded systems; industry of the future, production systems, and environment, management and business sciences.

Grenoble INP - UGA is an equal opportunity employer committed to sustainability. Grenoble INP-UGA celebrates diversity and equity and is committed to creating an inclusive environment for all employees. All qualified applications will be considered without discrimination of any kind.

Teaching

School : Grenoble INP - Phelma

School website: https://phelma.grenoble-inp.fr/

Contact : patrice.petitclair@phelma.grenoble-inp.fr

Grenoble INP Phelma is an engineering school within the Grenoble Institute of Engineering and Management. The school offers its students a wide range of courses at the cutting edge of scientific and technological progress: micro and nanotechnology, instrumentation, energy, innovative materials, information technology, biomedical engineering, process engineering, and environmental engineering. Phelma provides learning to more than 1,400 students in 11 different engineering programs, one of which is an apprenticeship program, and a dozen master's programs. The teaching staff is composed of about 100 full professors, and over 300 part-time associate professors. The school operates on two sites: Minatec in Grenoble, and the university campus in Saint-Martin d'Hères. Phelma's three main pillars - physics, electronics, and materials - are firmly anchored in the school's mission. The school's engineering and master's programs are evolving to keep pace with the changing needs of the industry, especially in the areas of energy and digital transition.

Teaching profile:

Embedded microelectronics and electronics represent about 25% of the science courses taught at Phelma, from transistors to embedded systems, including logic circuits, computer architectures, memories, and embedded computing. The candidate will teach VLSI digital microelectronics on ASIC and FPGA targets, hardware modeling languages (SystemVerilog, VHDL, etc.), system and circuit-level design flows, and the design of optimized and energy-efficient circuits and architectures for embedded systems. The open position will also be involved in the first year analog electronics courses (traditional and apprenticeship training), and in the Integrated Electronic Systems (SEI), Embedded Systems and Connected Objects (SEOC), Signal Images Communication and Multimedia (SICOM, joint course with Ense3) and the Microelectronics Telecoms (MT) apprenticeship course.

Since hands-on learning is an important part of Phelma's curriculum, the candidate will be expected to teach a significant portion of the courses in the context of lab works and projects.

Research

Host laboratory: SPINTEC (UMR 8191 Grenoble-INP, UGA, CEA and CNRS)

Laboratory website : http://www.spintec.fr/

Contacts : direction.spintec@cea.fr

SPINTEC is an academic research laboratory in spintronics, dedicated to the production of new fundamental knowledge, to its optimization and shaping for the purpose of innovation for industry. Its hallmarks are high-level publications, an active intellectual property policy, and strong academic and industrial partnerships. Created in 2002 and associated to Grenoble INP, UGA, CEA and CNRS, the laboratory now has more than a hundred employees, making

it one of the three largest spintronics laboratories worldwide. The laboratory has contributed to key discoveries in industrial spintronics, such as magnetic anisotropy at metal-oxide interfaces and spin-orbit couples at interfaces, and has successfully spun off four start-ups, with three others at various stages of development. The laboratory is strongly invested in education through research, starting about ten new PhD students yearly, and supporting several major international schools.

Research Profile: Design of spintronic circuits for artificial intelligence

The last decade has brought the emergence of numerous studies around embedded technologies for the fields of Big Data and Embedded Artificial Intelligence, with several application domains, ranging from the Internet of Things, to components for energy, health and environment, automotive and space. However, in order to enable the massive but rational use of these technologies, breakthrough innovations are required to achieve a better compromise between computing power and electricity consumption. One key factor is to rethink computing architectures to overcome the limitations inherent in the classic Von-Neumann computing model. The general idea is to bring the computation closer to the data to be processed by moving it to the peripheral circuits of memories (Near-Memory Computing), or even integrating it directly into the memory (In-Memory Computing). The time required to access the memory during calculation operations is consequently considerably decreased, reducing latency times and non-productive energy losses.

The promising and versatile characteristics of spintronic technologies allow considering a particularly efficient implementation of emerging architectures for artificial intelligence. Indeed, the intrinsic non-linearity and retention tuning of these devices offer a unique possibility to design low-power unconventional computing architectures (such as embedded neuromorphic architectures). The underlying building block devices can be classical spintronic devices (MRAM) or more emerging ones (hybrid ferroelectric – spintronic structures, skyrmions or “superparamagnetic tunnel junctions”.). SPINTEC has major assets in the development of these new concepts, combining in the same place all required expertise: materials development, nanofabrication, electrical tests, theoretical and simulation understanding of the spintronic phenomena involved, up to their integration in demonstrators. This has resulted in the laboratory's involvement in several large-scale projects: a dedicated chair at the Grenoble Institute of Artificial Intelligence (MIAI), the international ANR-DFG NEUSPIN and ANR-NSF STOCHASPIN projects, as well as participation as a key partner in the Electronics, Spin and AI PEPR national projects, which will start in the coming months.

Description of the research axes for this position

The candidate will be part of the "spintronics IC design" team and will bring complementary expertise in circuit design. The objective is to create a holistic chain of competencies, covering all the levels of abstraction of microelectronics, such as allowing the implementation of the design/validation flow specific to spintronics AI, from the circuit level to the architecture and system level (models, physical and statistical exploration tools, design/synthesis and fast simulation of circuits and architectures, PDK...). The position will be positioned at the interface between Artificial Intelligence and Device teams in the laboratory.

The research activities will focus on the aspects where spintronics shows key strengths. Memory computing will occupy a privileged place, as much for its importance in the current evolutions of computing architectures as for its adequacy with spintronics, the resistive nature of magnetic devices allowing an "analog" implementation of system features. The study of these new computing modes requires a study at the circuit level, but also at the system level, as the corresponding architectures are not directly compatible with conventional system architectures, nor with the corresponding standard tools. Independently of the design level considered, the intrinsic variabilities of such emerging technologies must be specifically taken into account. The objective will be to design the building blocks of such hardware accelerator architectures in a systematic way, but also to bring them up in a design flow in order to incorporate them into a complete computing system.

The candidate will have a sound understanding of circuit and architecture design and validation. Their skills will primarily include the highest levels of abstraction in microelectronics, the implementation of the design flow and the validation of architectures and systems, while having a good knowledge of integrated circuits at the full custom level. Their contribution will diversify the many existing collaborations with laboratories at national (LIRMM, INL, IM2NP, CNRS-Thales, EMSE, C2N, etc.) and international (KIT, Univ of Maryland, Univ Purdue, TU Dresden, Univ. Newcastle,

IHP Microelectronics) and industrial partners (TowerJazz, TRAD, Greenwaves, ST Microelectronics, Tiempo IC, Dolphin, Idemia, Antaios, Electronic Marin...).

Position assigned to a restricted area: NO

(Device for the protection of the scientific and technical potential of the nation, conditioning the appointment of the lecturer-researcher is subject to the authorization of the Defense Security Officer).

Specific requirements or conditions

Proficiency in English is required, as a number of the school's courses are provided only in English. In addition, international experience will be a decisive asset.

Administrative activities

In the mean term, the candidate recruited will have to take on responsibilities such as the coordination of Teaching Units or the management of Practical Labs and Platforms.

Specifics of the position

The courses may be given at the school's 2 locations: Grenoble and St Martin-d'Hères.

How to apply

Applicants must submit their applications on the GALAXIE Platform of the French Ministry of Higher Education and Research from the 23rd of February 2023, 10 a.m. (Paris time) to 30th of March 2023, 4 p.m. (Paris time).

Any document sent outside the GALAXIE procedure will not be taken into account.

The interview will include simulation/situational exercises. The details will be communicated when the invitation is sent out. In addition, part of the interview may be conducted in English.